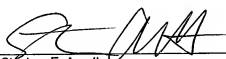


<b>TRANSMITTAL OF APPEAL BRIEF</b>			Docket No. 108298744US
In re Application of: Hiatt et al.			
Application No. 10/733,226-Conf. #8010	Filing Date December 10, 2003	Examiner C. A. Matthews	Group Art Unit 3754
Invention: MICROELECTRONIC DEVICES AND METHODS FOR FILLING VIAS IN MICROELECTRONIC DEVICES			
<b><u>TO THE COMMISSIONER OF PATENTS:</u></b>			
Transmitted herewith is the Appeal Brief in this application, with respect to the Notice of Appeal filed: <u>May 8, 2007</u> .			
The fee for filing this Appeal Brief is <u>\$ 500.00</u> .			
<input checked="" type="checkbox"/> Large Entity <input type="checkbox"/> Small Entity			
<input type="checkbox"/> A petition for extension of time is also enclosed.			
The fee for the extension of time is _____.			
<input checked="" type="checkbox"/> Payment in the amount of <u>\$ 500.00</u> is submitted by electronic funds transfer.			
<input type="checkbox"/> Charge the amount of the fee to Deposit Account No. <u>50-0665</u> . This sheet is submitted in duplicate.			
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.			
<input checked="" type="checkbox"/> The Director is hereby authorized to charge any additional fees that may be required or credit any overpayment to Deposit Account No. <u>50-0665</u> .			
 _____ Stephen E. Arnett Attorney Reg. No. : 47,392 PERKINS COIE LLP P.O. Box 1247 Seattle, Washington 98111-1247 (206) 359-8000		Dated: <u>July 9, 2007</u>	

(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

---

In re Patent Application of:  
Hiatt et al.

Application No.: 10/733,226

Confirmation No.: 8010

Filed: December 10, 2003

Art Unit: 3754

For: MICROELECTRONIC DEVICES AND  
METHODS FOR FILLING VIAS IN  
MICROELECTRONIC DEVICES

---

Examiner: C. A. Matthews

**APPEAL BRIEF**

MS Appeal Brief - Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

As required under § 41.37(a), this brief is filed within two months of the Notice of Appeal filed in this case on May 8, 2007, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

- |      |   |
|------|---|
| I.   | Real Party In Interest                        |
| II.  | Related Appeals and Interferences             |
| III. | Status of Claims                              |
| IV.  | Status of Amendments                          |
| V.   | Summary of Claimed Subject Matter             |
| VI.  | Grounds of Rejection to be Reviewed on Appeal |

VII.	Argument
VIII.	Claims Appendix
IX.	Evidence Appendix
X.	Related Proceedings Appendix

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Micron Technology, Inc.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which may be related to, directly affect, or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 39 claims pending in the application.

B. Current Status of Claims

1. Claims canceled: 15-27
2. Claims withdrawn from consideration but not canceled: 12-14 and 37
3. Claims pending: 1-14 and 28-52
4. Claims allowed: none
5. Claims rejected: 1-11, 28-36 and 38-52

C. Claims on Appeal

The claims on appeal are claims 1-11, 28-36 and 38-52.

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment After Final Rejection.

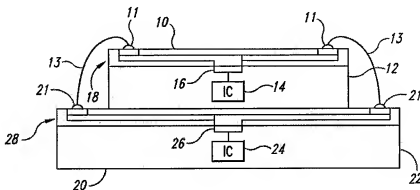
## V. SUMMARY OF CLAIMED SUBJECT MATTER

Conventional packaged microelectronic devices can include a singulated microelectronic die, an interposer substrate or lead frame attached to the die, and a moulded casing around the die. (Specification at ¶ [0003].) The die generally includes an integrated circuit and a plurality of bond-pads coupled to the integrated circuit. (*Id.*) The bond-pads are typically coupled to terminals on the interposer substrate or lead frame, and serve as external electrical contacts on the die through which supply voltage, signals, etc., are transmitted to and from the integrated circuit. (*Id.*) In addition to the terminals, the interposer substrate can also include ball-pads coupled to the terminals by conductive traces supported in a dielectric material. (*Id.*) Solder balls can be attached to the ball-pads in one-to-one correspondence to define a "ball-grid array." (*Id.*) Packaged microelectronic devices with ball-grid arrays are generally higher grade packages having lower profiles and higher pin counts than conventional packages using lead frames. (*Id.*)

Packaged microelectronic devices such as those described above are used in cellphones, pagers, personal digital assistants, computers, and many other electronic products. (Specification at ¶ [0007].) To meet the demand for smaller electronic products, there is a continuing drive to increase the performance of packaged microelectronic devices, while at the same time reducing the height and the surface area or "footprint" of such devices on printed circuit boards. (*Id.*) Reducing the size of high performance devices, however, is difficult because the sophisticated integrated circuitry requires more bond-pads, which results in larger ball-grid arrays and thus larger footprints. (*Id.*) One technique for increasing the component density of microelectronic devices within a given footprint is to stack one device on top of another. (*Id.*)

Figure 1 (reproduced below) schematically illustrates a first microelectronic device 10 attached to a second microelectronic device 20 in a wire-bonded, stacked-die arrangement. (Specification at ¶ [0008] and Figure 1) The first microelectronic device 10 includes a die 12 having an integrated circuit 14 electrically coupled to a series of bond-pads 16. (*Id.*) A redistribution layer 18 electrically couples a plurality of first solder balls 11 to corresponding bond-pads 16. (*Id.*) The second microelectronic device 20 similarly includes a die 22 having an integrated circuit 24 electrically coupled to a series of bond-pads 26. (*Id.*) A redistribution layer 28

electrically couples a plurality of second solder balls 21 to corresponding bond-pads 26. (*Id.*) Wire-bonds 13 extending from the first solder balls 11 to the second solder balls 21 electrically couple the first microelectronic device 10 to the second microelectronic device 20. (*Id.*)



**Fig. 1**  
(*Prior Art*)

The second solder balls 21 on the second microelectronic device 20 are positioned outboard of the first microelectronic device 10 to facilitate installation of the wire-bonds 13. (Specification at ¶ [0009] and Figure 1.) However, one drawback of positioning the second solder balls 21 in this manner is that it undesirably increases the footprint of the stacked-die arrangement. (See Specification ¶ [0009].) Another drawback is that installation of the wire-bonds 13 can be a complex and/or expensive process because it requires placing individual wires between each pair of solder balls. (*Id.*) Another drawback is that this type of installation may not be feasible for the high-density, fine-pitch arrays of some high-performance devices because the solder balls are not spaced apart far enough to be connected to individual wire-bonds. (*Id.*)

#### A. Claim 1

Claim 1 is directed to a method of forming a conductive interconnect in a microelectronic device in accordance with an embodiment of the invention. Claim 1 comprises, *inter alia*, providing a microfeature workpiece having a plurality of dies, and forming a passage extending through the microfeature workpiece from a first side of the microfeature workpiece to an opposite second side of the microfeature workpiece. (See, e.g., Specification at ¶¶ [0025]-[0027] and Figures

2 and 3.) The method further comprises forming a conductive plug in the passage adjacent to the first side of the microelectronic workpiece, and depositing conductive material in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece. (*See, e.g.*, Specification at ¶¶ [0031] and [0032] and Figures 5A and 5B.)

B. Claim 28

Claim 28 is directed to a packaged microelectronic device in accordance with an embodiment of the invention. Claim 28 comprises, *inter alia*, a die having a first side, a second side opposite to the first side and an integrated circuit positioned between the first and second sides. (*See, e.g.*, Specification at ¶ [0025] and Figures 2 and 3.) The packaged microelectronic device further comprises a bond-pad that is positioned on the first side of the die and that is electrically coupled to the integrated circuit, and a passage extending completely through the die and aligned with the bond-pad. (*See, e.g.*, Specification at ¶¶ [0025]-[0027] and Figures 2 and 3.) The packaged microelectronic device further comprises a first conductive material deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad. (*See, e.g.*, Specification at ¶ [0031] and Figure 5A.) The packaged microelectronic device further comprises a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die. (*See, e.g.*, Specification at ¶ [0032] and Figure 5B.)

C. Claim 33

Claim 33 is directed to a microfeature workpiece in accordance with an embodiment of the invention. Claim 33 comprises, *inter alia*, at least one die and a passage extending completely through the die from a first side of the microfeature workpiece to a second side of the microfeature workpiece. (*See, e.g.*, Specification at ¶¶ [0025] and [0027] and Figures 2 and 3.) The microfeature workpiece further comprises a first conductive material deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug and a second conductive material deposited in a second portion of the passage. (*See, e.g.*, Specification at ¶¶

[0031] and [0032] and Figures 5A and 5B.) The second conductive material is in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece. (*Id.*)

D. Claim 39

Claim 39 is directed to a microelectronic device set in accordance with an embodiment of the invention. Claim 39 comprises, *inter alia*, a first microelectronic device and at least a second microelectronic device. (*See, e.g.*, Specification at ¶ [0025] and Figure 2.) The first microelectronic device has a first die with a first integrated circuit, a first bond-pad electrically coupled to the first integrated circuit, and a passage extending completely through the first die and the first bond-pad. (*See, e.g.*, Specification at ¶¶ [0025] and [0027] and Figures 2 and 3.) The first microelectronic device further has a conductive interconnect deposited in the passage that includes a first conductive material deposited in a first portion of the passage to form a conductive plug and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage. (*See, e.g.*, Specification at ¶¶ [0031] and [0032] and Figures 5A and 5B.) The second microelectronic device has a second die with a second integrated circuit and a second bond-pad electrically coupled to the second integrated circuit. (*See, e.g.*, Specification at ¶ [0025] and Figure 2.) The second bond-pad is electrically coupled to the conductive interconnect of the first microelectronic device. (*See, e.g.*, Specification at ¶¶ [0008] and [0025] and Figure 2.)

E. Claim 44

Claim 44 is directed to a microelectronic device set in accordance with an embodiment of the invention. Claim 44 comprises, *inter alia*, a first microelectronic device and at least a second microelectronic device. (*See, e.g.*, Specification at ¶ [0025] and Figure 2.) The first microelectronic device has a first die with a first integrated circuit, a first bond-pad electrically coupled to the first integrated circuit and a passage aligned with the first bond-pad. (*See, e.g.*, Specification at ¶¶ [0025] and [0027] and Figures 2 and 3.) The first microelectronic device further has a conductive interconnect deposited in the passage that includes a first conductive material deposited in a first

portion of the passage to form a conductive plug in contact with the bond-pad and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage. (*See, e.g.*, Specification at ¶¶ [0031] and [0032] and Figures 5A and 5B.) The second microelectronic device has a second die with a second integrated circuit and a second bond-pad electrically coupled to the second integrated circuit. (*See, e.g.*, Specification at ¶ [0025] and Figure 2.) The second bond-pad is electrically coupled to the first bond-pad of the first microelectronic device. (*See, e.g.*, Specification at ¶¶ [0008] and [0025] and Figure 2.)

#### VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- A. Whether related U.S. Patent Application No. 10/713,878 was properly incorporated by reference;
- B. Whether claims 1, 6-11, 28-30, 33, 36, 38-42, 44, 45 and 48-52 are anticipated by U.S. Patent No. 6,703,310 to Mashino et al. ("Mashino") under 35 U.S.C. § 102(e);
- C. Whether claim 2 is unpatentable over Mashino in view of U.S. Patent No. 7,045,015 to Renn et al. ("Renn") under 35 U.S.C. § 103(a);
- D. Whether claims 3, 31, 34 and 46 are unpatentable over Mashino in view of U.S. Patent Application Publication No. 2004/0087441 to Hiramata et al. ("Hiramata") under 35 U.S.C. § 103(a);
- E. Whether claims 4, 32, 35 and 47 are unpatentable over Mashino in view of U.S. Patent Application Publication No. 2004/0087441 to Bock et al. ("Bock") under 35 U.S.C. § 103(a);
- F. Whether claim 5 is unpatentable over Mashino in view of U.S. Patent No. 6,828,223 to Chuang ("Chuang") under 35 U.S.C. § 103(a); and
- G. Whether claim 43 is unpatentable over Mashino in view of Applicant's Admitted Prior Art (APA) under 35 U.S.C. § 103(a).

#### VII. ARGUMENT

- A. Related U.S. Patent Application 10/713,878 was properly incorporated by reference

In the Final Office Action mailed on January 30, 2007 ("Final Office Action"), the Examiner stated that Applicant's incorporation by reference of related U.S. Patent Application No. 10/713,878 ("the incorporation by reference") was ineffective, allegedly because the related application's application number was not provided in paragraph [0001] of the Specification. (Final Office Action



at page 2.) The Examiner is incorrect. Related U.S. Patent Application No. 10/713,878 was properly incorporated by reference for at least two reasons. First, the incorporation by reference in the Specification as filed met the requirements of 37 C.F.R. § 1.57(b), which provides:

(b) Except as provided in paragraph (a) of this section, an incorporation by reference must be set forth in the specification and must:

- (1) Express a clear intent to incorporate by reference by using the root words "incorporat(e)" and "reference" (e.g., "incorporate by reference"); and
- (2) Clearly identify the referenced patent, application, or publication.

37 C.F.R. § 1.57(b). In the present case, the incorporation by reference was set forth in paragraph [0001] of the Specification as filed and expressed a clear intent to incorporate by reference by using the phrase "filed concurrently herewith and *incorporated* herein in its entirety by *reference*." (Specification as filed at ¶ [0001], emphasis added.) The incorporation by reference also clearly identified the related U.S. Patent Application by including three identifying pieces of information: 1) the Attorney Docket No. (10829.8742US00); 2) the Micron Disclosure Numbers (03-0599 and 03-0613); and 3) the title (MICROELECTRONIC DEVICES, METHODS FOR FORMING VIAS IN MICROELECTRONIC DEVICES, AND METHODS FOR PACKAGING MICROELECTRONIC DEVICES). Therefore, the incorporation by reference in the Specification as filed met the requirements of 37 C.F.R. § 1.57(b).

The related U.S. Patent Application was properly incorporated for a second reason, namely, Applicant filed a Preliminary Amendment on March 10, 2004 ("Preliminary Amendment") that amended paragraph [0001] of the Specification to include the application number and filing date of the U.S. Patent Application 10/713,878. More specifically, paragraph [0001] was amended to state:

This application is related to U.S. Patent Application No. 10/713,878 entitled MICROELECTRONIC DEVICES, METHODS FOR FORMING VIAS IN MICROELECTRONIC DEVICES, AND METHODS FOR PACKAGING MICROELECTRONIC DEVICES, filed November 13, 2003, and incorporated herein in its entirety by reference.

(Preliminary Amendment at page 2.) Because the incorporation by reference 1) expressed a clear intent to incorporate by reference related U.S. Patent Application No. 10/713,878 and 2) clearly identified this application, the incorporation by reference in amended paragraph [0001] of the Specification also met the requirements of 37 C.F.R. § 1.57(b), above. Paragraph [0027] was also amended to include the application number and filing date of related U.S. Patent Application 10/713,878. (*Id.*) For at least these reasons, related U.S. Patent Application No. 10/713,878 was properly incorporated by reference. Therefore, the Board should reverse this objection to the Specification.

B. Claims 1, 6-10, 28-30, 33, 36, 38-42, 44, 45 and 48-52 are not anticipated by Mashino under Section 102(e)

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631; 2 U.S.P.Q.2d (BNA) 1051, 1053 (Fed. Cir. 1987); M.P.E.P. § 2131 (8th Ed. 2001). Furthermore, an examiner has the burden of establishing a *prima facie* basis to defeat the patentability of a claim. *E.g., Ex parte Levy*, 17 U.S.P.Q.2d (BNA) 1461, 1462 (Bd. Pat. App. & Interf. 1990) ("it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."). Thus, to establish that a claim is anticipated by Mashino, the Examiner must show that each and every element, as set forth in the claim, is expressly or inherently described in Mashino.

The Examiner cannot establish a *prima facie* basis to defeat the patentability of claims 1, 6-10, 28-30, 33, 36, 38-42, 44, 45 and 48-52 because the Examiner cannot show that Mashino describes, either expressly or inherently, each and every element of these claims. For example, each of the independent claims 1, 28, 33, 39 and 44 recite, *inter alia*, a "conductive plug." As explained in further detail below, Mashino fails to describe this feature, and the other applied references fail to cure this deficiency. Therefore, Mashino cannot support a 35 U.S.C. § 102(e) rejection of the independent claims 1, 28, 33, 39 and 44. Accordingly, the Board should reverse the rejections of independent claims 1, 28, 33, 39 and 44 and corresponding dependent claims 6-10, 29, 30, 36, 38, 40-42, 45 and 48-52.

1. Claims 1, 6-11 and 48

In the Final Office Action, the Examiner asserted that Mashino discloses "forming a conductive plug." (Final Office Action at page 3, ¶ 3.) As set forth in detail below, however, Mashino does not describe forming a conductive plug as recited in claim 1.

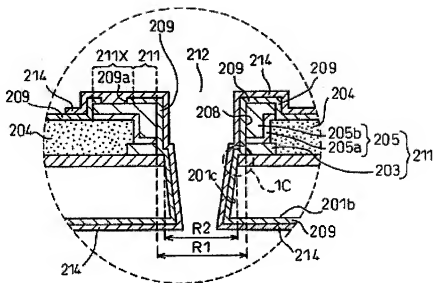
a. Claim 1 is Directed to a Method of Forming a Conductive Interconnect in a Microelectronic Device that Includes, *inter alia*, Forming a Conductive Plug in a Passage Adjacent to a First Side of a Microelectronic Workpiece

As discussed above in Section V.A, claim 1 is directed to a method of forming a conductive interconnect in a microelectronic device. The method includes, *inter alia*, forming a passage extending through a microfeature workpiece from a first side of the workpiece to a second side of the workpiece. The method further includes forming a conductive plug in the passage adjacent to the first side of the workpiece, and depositing conductive material in the passage to at least generally fill the passage from the conductive plug to the second side of the workpiece.

b. Mashino Discloses a Semiconductor Device Having a Conductive Film on the Inner Walls of a Through Hole

As shown in Figure 1B (reproduced below) of Mashino, this reference discloses a semiconductor device having a silicon substrate 201 with a through hole 212. (See Mashino at 6:44-7:5 and Figure 1B.)

Fig.1B



Insulating film 209 is formed on the inner walls of the through hole 212, and a conductive film referred to as an "interconnection pattern 214" is formed on the insulating film 209. (See Mashino at 6:3-5, 7:25-35 and Figure 1B.) As Mashino states, "in the illustrated example, the through hole 212 is hollow, but as shown in FIG. 7, it is also possible to fill the through hole 212 with a conductor 217 electrically connected with the interconnection pattern 214." (Mashino at 7:25-28.)

- c. Mashino Cannot Support a Section 102 Rejection of Independent Claim 1 for at Least the Reason that this Reference Fails to Disclose or Suggest Forming a Conductive Plug in a Passage Adjacent to a First Side of a Microelectronic Workpiece, and Depositing Conductive Material in the Passage to at Least Generally Fill the Passage From the Conductive Plug to a Second Side of the Workpiece

The method of claim 1 includes, *inter alia*, forming a passage from a first side of a microfeature workpiece to a second side of the workpiece, and forming a conductive plug in the passage adjacent to the first side of the workpiece. The method further includes depositing conductive material in the passage to at least generally fill the passage from the plug to the second



that it is also possible to fill the through hole 212 with a conductor 217, the interconnection pattern 214 still remains on the side walls of the through hole 212 only, and does not form a *plug* in the through hole 212.

In the Amendment filed on November 10, 2006 ("Amendment"), the Applicant argued that the interconnection pattern 214 could not reasonably be construed as the "conductive plug" of claim 1 because a plug is:

*1. An object, such as a cork, used to fill a hole tightly; a stopper. 2. A dense mass of material that obstructs a passage.* (The American Heritage College Dictionary, 3rd Edition 2000).

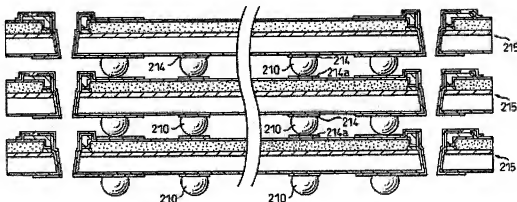
In response to the Applicant's argument, the Examiner stated that the interconnection pattern 214 could be construed as a conductive plug because a) the interconnection pattern 214 is a dense mass of material and b) since the provided second definition of a plug did not specify the degree to which a passage must be obstructed, the narrowing of the through hole 212 caused by the interconnection pattern 214 obstructed the through hole 212. (Final Office Action at page 13.)

The Applicant respectfully submits that the Examiner is engaging in semantic wordplay in construing the interconnection pattern 214 as a conductive plug. It is clear from Figures 1B and 7 of Mashino that the interconnection pattern 214 does not fill the through hole 212 tightly or act as a stopper. Even assuming, for the sake of argument, that the interconnection pattern 214 is a dense mass of material, it is clear from Figures 1B and 7 that it does not obstruct the through hole 212 to any measurable degree. If it were to obstruct the through hole 212, then the conductor 217 would not be able to fill the through hole 212, as shown in Figure 7. Therefore, the interconnection pattern 214 cannot reasonably be construed as the conductive plug of claim 1.

The Examiner incorrectly construes the interconnection pattern 214 as a conductive plug for at least one additional reason. Mashino's Figure 3 (reproduced below) illustrates a sectional view of a semiconductor module obtained by stacking a plurality of semiconductor devices 215. Mashino states that the solder bumps 210 function to electrically connect the interconnection patterns 214 of

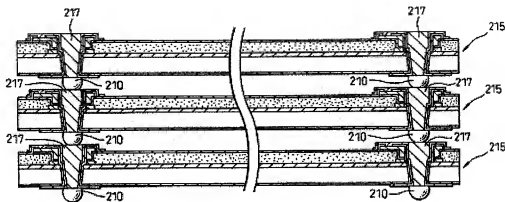
the semiconductor devices 215. (Mashino at 7:62-65.) As shown in Figure 3, the solder bumps 210 are offset from the through holes. If the Examiner was correct that the interconnection pattern 214 can be construed as a conductive plug, then the solder bumps 210 would be placed directly beneath the through holes to allow the semiconductor devices 215 to be more efficiently coupled.

Fig.3



As shown in Figure 8 of Mashino (reproduced below), however, the solder bumps 210 sit directly beneath the through holes only when the through holes have been filled with the conductors 217. Applicant submits that if the Examiner's position were correct, then the conductors 217 would be superfluous and there would be no need for the embodiment shown in Figure 8. However, this is clearly not the case, as the conductors 217 function to fill the through holes so that the solder bumps 210 can electrically couple the semiconductor devices 215. This is further evidence that the interconnection pattern 214 cannot reasonably be construed as a conductive plug.

Fig. 8



Accordingly, Mashino cannot support a Section 102 rejection of claim 1 for at least the reason that this reference fails to teach or suggest forming a conductive plug in a passage in a microfeature workpiece. Therefore, the rejection of claim 1 is improper and should be reversed.

Claims 6-10 and 48 depend from base claim 1. Accordingly, Mashino cannot support a Section 102 rejection of dependent claims 6-10 and 48 for at least the reason that this reference cannot support a Section 102 rejection of corresponding base claim 1, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 6-10 and 48 is improper and should be reversed.

## 2. Claims 28-30 and 49

As discussed above in Section V.B, independent claim 28 is directed to a packaged microelectronic device that includes features at least generally similar to features described above with reference to claim 1. For example, the device of claim 28 includes, *inter alia*, a passage extending completely through a die, and a first conductive material deposited in a first portion of the passage adjacent to a first side of the die to form a conductive plug. The device of claim 28 further includes a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to a second side of the die.



In rejecting claim 28, the Examiner asserted that Mashino discloses "a first conductive material (214) deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad; and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die." (Final Office Action at page 4, ¶ 10.) As discussed above with reference to the rejection of claim 1, however, Mashino fails to teach or suggest, at least, a first conductive material forming a conductive *plug* in a passage, and a second conductive material at least generally filling the passage *from the conductive plug* to a second side of the die. Therefore, Mashino cannot support a Section 102 rejection of claim 28 for at least this reason, and the rejection should be reversed.

Claims 29, 30 and 49 depend from base claim 28. Accordingly, Mashino cannot support a Section 102 rejection of dependent claims 29, 30 and 49 for at least the reason that this reference cannot support a Section 102 rejection of corresponding base claim 28, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 29, 30 and 49 is improper and should be reversed.

3. Claim 33, 36, 38 and 50

As discussed above in Section V.C, independent claim 33 is directed to a microfeature workpiece that includes, *inter alia*, features at least generally similar to those discussed above with reference to claim 1. For example, the microfeature workpiece of claim 33 includes, *inter alia*, a passage extending completely through a die from a first side of a microfeature workpiece to a second side of the microfeature workpiece. The microfeature workpiece further includes a first conductive material deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece *to form a conductive plug*. In addition, the microfeature workpiece also includes a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage *from the conductive plug* to the second side of the microfeature workpiece.

In rejecting claim 33, the Examiner asserts that Mashino discloses "a first conductive material (214) deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug; and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece." (Final Office Action at p. 5, ¶ 13.) As set forth above, however, Mashino does not describe, at least, the first and second conductive materials of claim 33. Therefore, the rejection of claim 33 is improper and should be reversed.

Claims 36, 38 and 50 depend from base claim 33. Accordingly, Mashino cannot support a Section 102 rejection of dependent claims 36, 38 and 50 for at least the reason that this reference cannot support a Section 102 rejection of corresponding base claim 33, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 36, 38 and 50 is improper and should be reversed.

4. Claims 39-42 and 51

As discussed above in Section V.D, independent claim 39 is directed to a microelectronic device set that includes a first microelectronic device having, *inter alia*, features that are at least generally similar to features discussed above with reference to claim 1. The features include, *inter alia*, a first conductive material deposited in a first portion of a passage *to form a conductive plug*, and a second conductive material deposited in a second portion of the passage *in contact with the conductive plug* to at least generally fill the passage.

In rejecting claim 39, the Examiner asserted that Mashino discloses a "conductive interconnect including a first conductive material (214) deposited in a first portion of the passage to form a conductive plug, and a second conductive material (217) deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage." (Final Office Action at page 6, ¶ 16.) However, for at least the reasons set forth above, Applicant submits that Mashino fails to describe these features. Therefore, the rejection of claim 39 is improper and should be reversed.

Claims 40-42 and 51 depend from base claim 39. Accordingly, Mashino cannot support a Section 102 rejection of dependent claims 40-42 and 51 for at least the reason that this reference cannot support a Section 102 rejection of corresponding base claim 39, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 40-42 and 51 is improper and should be reversed.

5. Claims 44, 45 and 52

As discussed above in Section V.E, independent claim 44 is directed to a microelectronic device set that includes, *inter alia*, features at least generally similar to the features discussed above with reference to independent claim 39. Therefore, claim 44 distinguishes over the Mashino reference for at least the reasons discussed above with reference to independent claim 39, and the rejection of claim 44 is improper and should be reversed.

Claims 45 and 52 depend from base claim 44. Accordingly, Mashino cannot support a Section 102 rejection of dependent claims 45 and 52 for at least the reason that this reference cannot support a Section 102 rejection of corresponding base claim 44, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 45 and 52 is improper and should be reversed.

C. Claim 2 is patentable over Mashino in view of Renn under 35 U.S.C. § 103(a)

Claim 2 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mashino in view of Renn. Claim 2 depends from base claim 1. As discussed in detail above in Section VII.B, Mashino fails to describe each and every element as set forth in claim 1. For example, Mashino fails to teach or suggest the conductive plug of claim 1. Furthermore, Renn fails to cure this and other deficiencies of Mashino with respect to claim 1. Accordingly, the combination of Mashino and Renn cannot support a Section 103 rejection of dependent claim 2 for at least the reasons that these references cannot support a Section 103 rejection of corresponding base claim 1, and for the additional features of this dependent claim. Therefore, the rejection of dependent claim 2 is improper and should be reversed.

D. Claims 3, 31, 34 and 46 are patentable over Mashino in view of Hirakata under 35 U.S.C. § 103(a)

Claims 3, 31, 34 and 46 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mashino in view of Hirakata. Claim 3 depends from base claim 1, claim 31 depends from base claim 28, claim 34 depends from base claim 33, and claim 46 depends from base claim 44. As discussed in detail above in Section VII.B, Mashino cannot support a Section 102 rejection of base claims 1, 28, 33 and 44 for at least the reason that this reference fails to describe each and every element as set forth in these claims. Furthermore, Hirakata fails to cure the deficiencies of Mashino with regard to base claims 1, 28, 33 and 44. Accordingly, the combination of Mashino and Hirakata cannot support a Section 103 rejection of dependent claims 3, 31, 34 and 46 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claims 1, 28, 33 and 44, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 3, 31, 34 and 46 is improper and should be reversed.

E. Claims 4, 32, 35 and 47 are patentable over Mashino in view of Bock under 35 U.S.C. § 103(a)

Claims 4, 32, 35 and 47 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mashino in view of Bock. Claim 4 depends from base claim 1, claim 32 depends from base claim 28, claim 35 depends from base claim 33, and claim 47 depends from base claim 44. As discussed in detail above in Section VII.B, Mashino cannot support a Section 102 rejection of base claims 1, 28, 33 and 44 for at least the reason that this reference fails to describe each and every feature as set forth in these claims. Furthermore, Bock fails to cure the deficiencies of Mashino with respect to base claims 1, 28, 33 and 44. Accordingly, the combination of Mashino and Bock cannot support a Section 103 rejection of dependent claims 4, 32, 35 and 47 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claims 1, 28, 33 and 44, and for the additional features of these dependent claims. Therefore, the rejection of dependent claims 4, 32, 35 and 47 is improper and should be reversed.

F. Claim 5 is patentable over Mashino in view of Chuang under 35 U.S.C. § 103(a)

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mashino in view of Chuang. Claim 5 depends from base claim 1. As set forth above in Section VII.B, Mashino fails to describe each and every element as set forth in claim 1. Furthermore, Chuang fails to cure the deficiencies of Mashino with respect to base claim 1. Therefore, the combination of Mashino and Chuang cannot support a Section 103 rejection of dependent claim 5 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claim 1, and for the additional features of this dependent claim. Therefore, the rejection of dependent claim 5 is improper and should be reversed.

G. Claim 43 is patentable over Mashino in view of APA under 35 U.S.C. § 103(a)

Claim 43 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Mashino in view of the APA. Claim 43 depends from base claim 39. As set forth in detail above in Section VII.B, Mashino fails to describe each and every element as set forth in base claim 39. Furthermore, the APA fails to cure the deficiencies of Mashino with respect to base claim 39. Accordingly, the combination of Mashino and the APA cannot support a Section 103 rejection of dependent claim 43 for at least the reason that these references cannot support a Section 103 rejection of corresponding base claim 39, and for the additional features of this dependent claim. Therefore, the rejection of dependent claim 43 is improper and should be reversed.

H. Conclusion

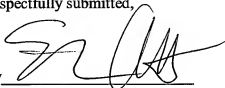
Each of claims 1-11, 28-36 and 38-52 has been improperly rejected for at least the reason that the applied references, either singularly or in combination, fail to describe each and every element of the pending claims. Accordingly, the Board should reverse the rejections of the pending claims.

The Director is hereby authorized to charge any deficiency in the fees filed to Deposit Account No. 50-0665, under Order No. 108298744US from which the undersigned is authorized to draw.

Dated:

July 9, 2007

Respectfully submitted,



By

Stephen E. Arnett

Registration No.: 47,392

PERKINS COIE LLP

P.O. Box 1247

Seattle, Washington 98111-1247

(206) 359-8000

(206) 359-7198 (Fax)

Attorney for Applicant

## VIII. CLAIMS APPENDIX

Claims Involved in the Appeal of Application Serial No. 10/733,226:

1. (Original) A method of forming a conductive interconnect in a microelectronic device, the method comprising:  
providing a microfeature workpiece having a plurality of dies;  
forming a passage extending through the microfeature workpiece from a first side of the microfeature workpiece to an opposite second side of the microfeature workpiece;  
forming a conductive plug in the passage adjacent to the first side of the microelectronic workpiece; and  
depositing conductive material in the passage to at least generally fill the passage from the conductive plug to the second side of the microelectronic workpiece.
2. (Original) The method of claim 1 wherein forming a conductive plug includes depositing an electrically conductive material in the passage using a maskless mesoscale materials deposition process.
3. (Original) The method of claim 1 wherein forming a conductive plug includes applying an electronic ink in the passage using an electronic printing process.
4. (Original) The method of claim 1 wherein forming a conductive plug includes depositing an electrically conductive material in the passage using a nano-particle deposition process.
5. (Original) The method of claim 1 wherein forming a conductive plug includes depositing silver in the passage.

6. (Original) The method of claim 1, further comprising forming a bond-pad on the microelectronic workpiece, wherein forming the passage includes forming the passage through the bond-pad, and wherein forming a conductive plug in the passage includes depositing a conductive material to contact an exposed surface of the bond-pad.

7. (Original) The method of claim 1 wherein forming the passage includes laser drilling the passage through the die.

8. (Original) The method of claim 1 wherein providing a microfeature workpiece includes providing a die having an integrated circuit and a bond-pad electrically coupled to the integrated circuit, and wherein forming the passage includes laser drilling the passage through the die and the bond pad.

9. (Original) The method of claim 1, further comprising applying a passivation layer to at least a portion of the passage before forming the conductive plug in the passage and filling the passage from the conductive plug to the second side of the microelectronic workpiece.

10. (Original) The method of claim 1, further comprising forming a bond-pad on the microelectronic workpiece in contact with the conductive plug.

11. (Original) The method of claim 1 wherein depositing conductive material in the passage to at least generally fill the passage includes biasing the conductive plug at an electrical potential.

12. (Withdrawn) The method of claim 1, further comprising forming a metallic layer on the first side of the microelectronic workpiece in contact with the conductive plug.

13. (Withdrawn) The method of claim 1, further comprising forming a metallic layer on the first side of the microelectronic workpiece in contact with the conductive plug, wherein



depositing conductive material in the passage to at least generally fill the passage includes biasing the metallic layer at an electrical potential.

14. (Withdrawn) The method of claim 1 wherein forming a conductive plug includes depositing an electrically conductive material in the passage using solder tent technology.

15-27. (Canceled)

28. (Original) A packaged microelectronic device comprising:

a die having a first side and a second side opposite to the first side, the die further having an integrated circuit positioned between the first and second sides;

a bond-pad positioned on the first side of the die and electrically coupled to the integrated circuit;

a passage extending completely through the die and aligned with the bond-pad;

a first conductive material deposited in a first portion of the passage adjacent to the first side of the die to form a conductive plug electrically connected to the bond-pad; and

a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the die.

29. (Original) The packaged microelectronic device of claim 28, further comprising an insulative layer deposited in the passage between the die and the first and second conductive materials.

30. (Original) The packaged microelectronic device of claim 28 wherein the passage extends through the bond-pad, and further comprising an insulative layer deposited in the passage between the die and the first and second conductive materials.

31. (Original) The packaged microelectronic device of claim 28 wherein the passage extends through the bond-pad, and wherein the first conductive material includes an electronic ink in contact with an exposed surface of the bond pad.

32. (Original) The packaged microelectronic device of claim 28 wherein the passage extends through the bond-pad, and wherein the first conductive material includes a nano-particle deposition in contact with an exposed surface of the bond pad.

33. (Original) A microfeature workpiece having a first side and a second side opposite to the first side, the microfeature workpiece comprising:

- at least one die;

- a passage extending completely through the die from the first side of the microfeature workpiece to the second side of the microfeature workpiece;

- a first conductive material deposited in a first portion of the passage adjacent to the first side of the microfeature workpiece to form a conductive plug; and

- a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage from the conductive plug to the second side of the microfeature workpiece.

34. (Original) The microfeature workpiece of claim 33 wherein the first conductive material includes an electronic ink.

35. (Original) The microfeature workpiece of claim 33 wherein the first conductive material includes a nano-particle deposition.

36. (Previously presented) The microfeature workpiece of claim 33, further comprising an insulative layer deposited in the passage between the die and the first and second conductive materials.

37. (Withdrawn) The microfeature workpiece of claim 33, further comprising a metallic layer formed on the first side of the microfeature workpiece.

38. (Original) The microfeature workpiece of claim 33, further comprising a bond-pad formed on the first side of the microfeature workpiece in contact with the conductive plug.

39. (Original) A microelectronic device set comprising:  
a first microelectronic device having:

- a first die with a first integrated circuit and a first bond-pad electrically coupled to the first integrated circuit, the first die further including a passage extending completely through the first die and the first bond-pad; and

- a conductive interconnect deposited in the passage, the conductive interconnect including a first conductive material deposited in a first portion of the passage to form a conductive plug, and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and

at least a second microelectronic device having a second die with a second integrated circuit and a second bond-pad electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the conductive interconnect of the first microelectronic device.

40. (Original) The microelectronic device set of claim 39 wherein the first microelectronic device is attached to the second microelectronic device in a stacked-die arrangement.

41. (Original) The microelectronic device set of claim 39, further comprising a solder ball disposed between the conductive interconnect of the first microelectronic device and the second bond-pad of the second microelectronic device to electrically couple the first bond-pad to the second bond-pad.

42. (Original) The microelectronic device set of claim 39 wherein the passage is a first passage, wherein the second microelectronic device further includes a second passage extending through the second die and the second bond-pad, and wherein the second passage is completely filled with a third conductive material.

43. (Original) The microelectronic device set of claim 39 wherein the first microelectronic device further includes a redistribution layer formed on the first die, the redistribution layer including a conductive line having a first end portion attached to the first bond-pad and a second end portion positioned outward of the first end portion, wherein the second end portion is configured to receive electrical signals and transmit the signals to at least the first integrated circuit of the first die and the second integrated circuit of the second die.

44. (Original) A microelectronic device set comprising:

a first microelectronic device having:

a first die with a first integrated circuit and a first bond-pad electrically coupled to the first integrated circuit, the first die further including a passage aligned with the first bond-pad; and

a conductive interconnect deposited in the passage, the conductive interconnect including a first conductive material deposited in a first portion of the passage to form a conductive plug in contact with the bond-pad, and a second conductive material deposited in a second portion of the passage in contact with the conductive plug to at least generally fill the passage; and

at least a second microelectronic device having a second die with a second integrated circuit and a second bond-pad electrically coupled to the second integrated circuit, wherein the second bond-pad is electrically coupled to the first bond-pad of the first microelectronic device.

45. (Previously presented) The packaged microelectronic device of claim 44, further comprising an insulative layer deposited in the passage between the first die and the first and second conductive materials.

46. (Original) The packaged microelectronic device of claim 44 wherein the passage extends through the first bond-pad, and wherein the first conductive material includes an electronic ink in contact with an exposed surface of the bond pad.

47. (Original) The packaged microelectronic device of claim 44 wherein the passage extends through the bond-pad, and wherein the first conductive material includes a nano-particle deposition in contact with an exposed surface of the bond pad.

48. (Previously presented) The method of claim 1, further comprising applying a passivation layer to at least a portion of the passage before forming the conductive plug in the passage, and wherein depositing conductive material in the passage to at least generally fill the passage includes depositing the conductive material in contact with the conductive plug and the passivation layer.

49. (Previously presented) The packaged microelectronic device of claim 28, further comprising an insulative layer deposited in the passage, wherein the second conductive material contacts the conductive plug and the insulative layer.

50. (Previously presented) The microfeature workpiece of claim 33, further comprising an insulative layer deposited in the passage, wherein the second conductive material contacts the conductive plug and the insulative material.

51. (Previously presented) The microelectronic device set of claim 39 wherein the first microelectronic device further includes an insulative layer deposited in the passage, and wherein the second conductive material contacts the conductive plug and the insulative layer.

52. (Previously presented) The microelectronic device set of claim 44 wherein the first microelectronic device further includes an insulative layer deposited in the passage, and wherein the second conductive material contacts the conductive plug and the insulative layer.

IX. EVIDENCE APPENDIX

The American Heritage College Dictionary (3d ed. 2000) definition of "plug" is being provided. This evidence was referenced in the Amendment at page 12 and entered in the record by the Examiner.

THE  
AMERICAN  
HERITAGE®  
COLLEGE  
DICTIONARY

---

THIRD EDITION

*n·a·r·y*



HOUGHTON MIFFLIN COMPANY

*Boston • New York*



**pliable** (plī-ə) *v.* **pliable**, **pliable**, **pliable**. — *intr.* 1. To fall with a sound like that of an object falling into water without splashing. 2. To let the body drop heavily. — *tr.* To drop or set heavily, with or as if with a **pliable**. — *n.* A pliable sound or movement. [imit. — **pliable** *adj.*]

**plio-sion** (plī-ō-shən) *n.* **Ling.** 1. The articulation of a plosive sound. 2. The sudden release of occluded air characteristic of plosives. [OE *pliosion*]

**plio-sive** (plī-ō-sīv) *adj.* **Ling.** — *adj.* Of or being a speech sound produced by complete closure of the oral passage and subsequent release with a burst of air, as in the sound (p) in **pit**. — *n.* A plosive speech sound. [OE *pliosion*]

**plot** (plɒt) *n.* 1. a. A small piece of ground, generally used for a specific purpose. b. A measured area of land, a box. 2. A ground plan, as for a building or a diagram. 3. See **graph** 1. 4. The pattern of events or main story in a narrative or drama. 5. A secret plan to accomplish a hostile or illegal purpose. — *v.* **plot**-ted, **plot**-ting, **plots**. — *tr.* 1. To represent graphically, as on a chart. 2. **Math.** a. To locate (points or other figures) on a graph by means of coordinates. b. To draw (a curve) connecting points on a graph. 3. To conceive and arrange the action and incidents of. 4. To form a plot for; prearrange secretly or deviously. — *intr.* 1. To be located by means of coordinates, as on a chart or with data. 2. To form or take part in a plot; scheme. [ME < OE]

**Plot** (plɒt) *n.* A movement in ballet in which the knees are held back in a bold straight. [Fr. < p. part of **plier**, to bend < OFr. See **nuver**.]

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

**Plot** (plɒt) *n.* P. and p. part of **ply**.

X. RELATED PROCEEDINGS APPENDIX

No related proceedings are referenced in Section II, above, and no copies of decisions in any related proceeding are being provided.